ABSTRACT OF THE DISCLOSURE

A non-volatile semiconductor memory device, comprising a memory cell array including a plurality of electrically erasable programmable non-volatile memory cells arrayed and divided into a plurality of blocks; a plurality of word lines arranged in each of said plurality of blocks and each commonly connected to memory cells on an identical row; a plurality of drive lines provided corresponding to said plurality of word lines and each arranged to supply a voltage to the corresponding word line; a plurality of transfer transistors each operative as a switch to connect the corresponding word line to the corresponding drive line among said plurality of word lines and said plurality of drive lines, wherein said plurality of word lines are classified into an arbitrary word line determined arbitrarily, secondary adjacent word lines located adjacent to both word lines adjacent to said arbitrary word line, and residual word lines other than said arbitrary word line and said secondary adjacent word lines, and wherein among said plurality of transfer transistors, transfer transistors for said residual word lines are arranged at both adjacent locations and an opposite location around a transfer transistor for said arbitrary word line.